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On the intrinsic limits of pentacene field-effect transistors

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Abstract

Performance limits for pentacene based field-effect transistors are investigated using single- and polycrystalline devices. Whereas the charge transport in single crystalline devices is band-like with mobilities up to 10^5 $cm^2/V\,s$ at low temperatures, temperature-independent or thermally activated charge transport can be observed in polycrystalline thin film transistors depending on the growth conditions. Trapping and grain boundary effects significantly influence the temperature dependence of the field-effect mobility. Furthermore, the device performance of p-channel transistors (mobility, on/off ratio, sub-threshold swing) decreases slightly with increasing trap densities. However, the formation of an electron accumulation layer (n-channel) is significantly stronger affected by trapping processes in the thin film devices. Single crystalline p-channel devices exhibit at room temperature mobilities as high as 3.2 $cm^2/V\,s$, on/off-ratios exceeding 10^9, and sub-threshold swings as low as 60 mV/decade. Slightly diminished values are obtained for transistors working as n-channel devices (2 $cm^2/V\,s$, 10^8, and 150 mV/decade).

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Keywords: Pentacene; Field-effect transistor; Mobility; Grain boundaries

1. Introduction

Organic field-effect transistors (FETs) have emerged as promising technology for low-cost electronics such as smart cards or identification tags [1–3]. Among all investigated oligomeric and polymeric materials, pentacene thin films have demonstrated the best electrical performance so far. Mobilities exceeding 1.5 $cm^2/V\,s$, on/off ratios of $>10^7$, and sub-threshold swings below 1 V/decade have been reported [4,5]. In addition, the use of high dielectric constant insulators results in low switching voltages for organic transistors [2,6]. High switching speeds can be achieved in complementary circuits in combination with amorphous silicon or organic n-channel materials [6–9]. In addition, ambipolar, i.e. p- as well as n-channel activity, operation of single crystalline devices has been observed and first complementary inverter circuits have been demonstrated [10].

In this study, we report on FETs based on pentacene single crystals as well as thin films, both prepared from the vapor phase. The charge transport in these devices is investigated in the temperature range from 2 to 300 K. The influence of traps, disorder, and grain boundaries in thin films is analyzed. Furthermore, performance limits, based on single crystal FET measurements, are discussed.

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2. Device preparation

Pentacene single crystals and thin films have been grown from the vapor phase in a stream of flowing gas. Details of the experimental technique for single crystal growth have been reported earlier [11]. A similar apparatus was used for the growth of thin films on polyimide substrates by organic vapor phase deposition. This technique is known to be capable of growing crystalline, high quality organic thin films [12,13]. In both processes, single crystal growth and thin film deposition, the evaporating material is heated up to 300°C in the first zone of a two-zone furnace. The second zone of the furnace is held at 200°C in the case of single crystals and near room temperature (no additional heating or cooling) for thin film deposition. However, inside the reactor the substrate (polyimide) is heated by the flow (100–140 ml/min) of hydrogen or forming gas ($N_2 + H_2$). All investigated thin film devices (TF1–4) were deposited in one run, with the distance between the substrate and the evaporation zone increasing from sample TF1 to TF4. Therefore, TF1 was grown at the highest temperature and TF4 at the lowest temperature.

Source and drain contacts as well as the gate electrode have been prepared by thermal evaporation of gold through a shadow mask. Typical channel length and width are in the range from 20 to 50 and 500 to 2000 μm, respectively. RF-magnetron sputtered amorphous Al_2O_3 of various thicknesses ($C_i \approx 30$–130 nF/cm^2) has been used as gate insulator. The schematic structure of the devices used in this study is shown in Fig. 1.

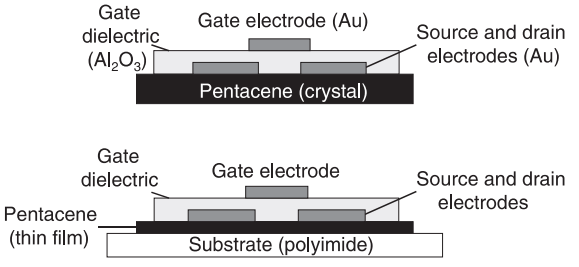

Fig. 1. Schematic structure of the single crystal (top) and thin film (bottom) FETs. Drain, source and gate electrodes were prepared by thermal evaporation of gold. The gate dielectric, amorphous Al_2O_3, was RF-magnetron sputtered.

3. Results

3.1. Single crystals

Fig. 2 shows the drain current I_d of a pentacene single crystal FET (SX) in hole accumulation (p-channel) as a function of drain V_d and gate voltage V_g. A field-effect mobility of 3.2 cm^2/V s at room temperature is deduced either from the linear or the saturation regime [14]. Furthermore, a sub-threshold swing S ($S = \ln 10 \partial V_g / \partial \ln I_d$) as steep as 60 mV/decade is observed (see Fig. 3) at room temperature, reflecting the low defect density of the single crystalline material and the high quality of the Al_2O_3/pentacene interface. Using standard FET-equations S can be expressed as [14]

$$S \cong \frac{kT}{e}\left(1 + \frac{C_D}{C_i}\right)\ln 10 \geqslant \frac{kT}{e}, \qquad (1)$$

where C_D is the space charge capacitance per unit area, which can arise from trapped charges or from doping of the crystal. The inset in Fig. 3 shows, that S is thermally limited down to approximately 100 K. This might be attributed to the high-quality interface due to the absence of dangling bond-type defects in van-der-Waals bonded materials.

Fig. 4 shows the field-effect mobility of device SX as function of temperature. In this configura-

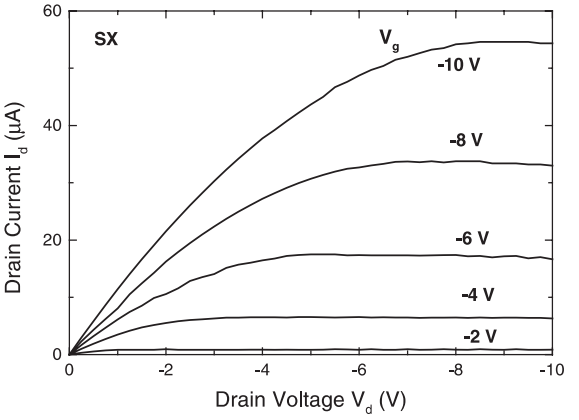

Fig. 2. Drain current versus drain voltage at various gate voltages for a p-channel pentacene single crystal transistor (SX) at room temperature.

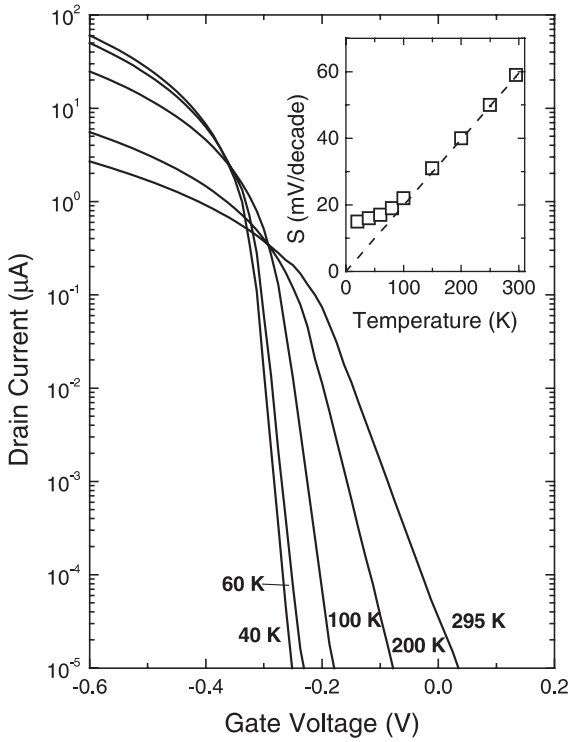

Fig. 3. Transfer characteristics of a p-channel pentacene single crystal transistor (SX) at temperatures between 40 and 295 K. The inset shows the sub-threshold swing as function of temperature. The dashed line corresponds to a thermally limited sub-threshold swing.

tion, the mobility of carriers near the interface between pentacene and the gate oxide is measured. The mobility increases up to 10^5 cm^2/V s at low temperatures following a power law ($T^{-2.7}$). The extremely high low temperature mobility in combination with the temperature dependence (power law) suggests coherent band-like charge transport of delocalized charge carriers in pentacene single crystal FETs. Thermally activated hopping can be ruled out definitively as intrinsic transport mechanism. The temperature dependence of the field-effect mobility compare well with values obtained from our previous bulk measurements (space-charge-limited-current measurements) on pentacene crystals [15] and with time-of-flight measurements on related materials like naphthalene or perylene [16,17].

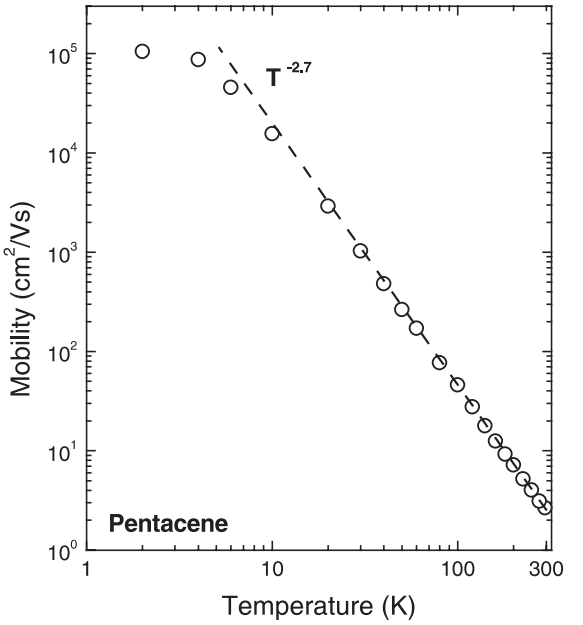

Fig. 4. Temperature dependence of the p-channel field-effect mobility of a pentacene single crystal transistor (SX).

3.2. Thin film devices

Fig. 5 shows the temperature dependence of the field-effect mobility of pentacene thin film FETs deposited at four different temperatures (TF1–4). A wide range of temperature dependences is observed comprising the various behaviors reported

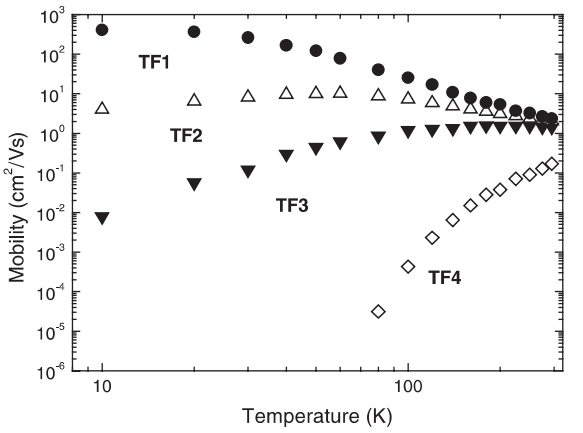

Fig. 5. Temperature dependence of the p-channel field-effect mobility of pentacene thin film transistors (TF1–4).

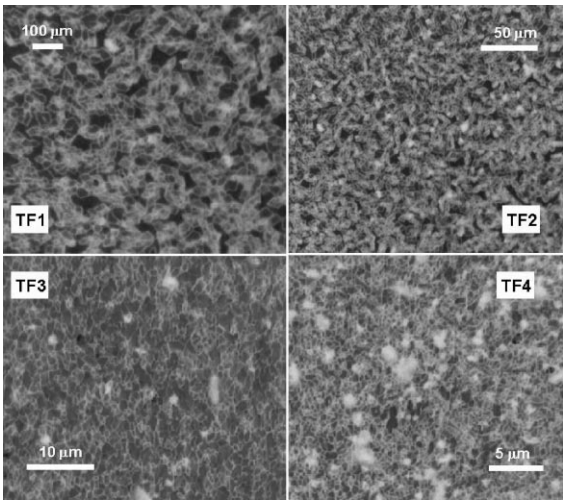

Fig. 6. Optical micrographs (crossed polarizers) of the morphology of thin films used for devices TF1–4.

previously [18]. Whereas device TF1 exhibits single crystalline-like charge transport (power law dependence), device TF4 reveals thermally activated transport. We find a systematic correlation between the electrical properties and the thin film morphology (see Fig. 6). In sample TF1 the grain sizes exceed the length of the transistor channel and thus the devices behave like a single crystalline thin film FET. With decreasing deposition temperature the grain size decreases for the polycrystalline devices TF2–4. Consequently grain boundary effects become more and more important in thin films TF2–4.

In general, the mobility μ in a polycrystalline material may be described as

$$\mu^{-1} = \mu_{GB}^{-1} + \mu_{B}^{-1}, \tag{2}$$

where μ_{GB} and μ_B are the 'grain boundary mobility' and the bulk (intragrain) mobility, respectively. The 'grain boundary mobility' in organic semiconductor thin films depends mainly on the barrier height at the grain boundary E_B, which is a function of the number of charged trapping states at the boundary, the carrier concentration within the grain, and the temperature.

$$\mu_{GB} = \mu_0 \exp\left(-\frac{E_B}{k_B T}\right), \tag{3}$$

where E_B is given by [19,20]

$$E_B = \frac{e n_t^2}{8\varepsilon_0 \varepsilon_r p}, \tag{4}$$

where p is the effective carrier density within the grain (which can be calculated above the threshold from the gate voltage and the gate capacitance), ε_r the relative dielectric constant, ε_0 the permittivity of the free space, and n_t the density of charge trapped in surface states, which can be expressed as [19]

$$n_t = \frac{N_t}{1 + \exp\left(\frac{E_t - E_F}{kT}\right)}, \tag{5}$$

where N_t is the area trap density, E_t the trap energy, and E_F the Fermi energy. In general, the single trap level at E_t may be replaced by a distribution of levels. However, this will result only in more complicated calculations, the basic physics, however, will remain unchanged. In the following we will assume the simplified case of a discrete trap level. We like to mention that trapped charge at grain boundaries might also lead to the formation of a potential well [21]. A similar thermally activated transport can be expected in this case. Moreover, a minimum of the mobility might be observed in such a case as reported for α-sexithiophene thin films [22] or polycrystalline silicon [23]. Since such a minimum is not observed in our pentacene devices, we focus on positively charged grain boundaries leading to the formation of a potential barrier.

In this model, the barrier height at the grain boundary E_B depends significantly on the number of trapping states at the boundary. Different thin film deposition conditions, therefore, may lead to different barrier heights and, thus, to very different temperature dependences of the field-effect mobility [18,21]. Furthermore E_B also varies with temperature depending on the energy position of the trap level E_t and the Fermi energy. Fig. 7 compares the measured field-effect mobilities of TF2–4 with model calculations. The 'grain boundary mobilities' μ_{GB} (calculated using Eqs. (1)–(4) and the mobility of TF1 as μ_B) and fitted mobilities μ are calculated assuming different trap densities (see Table 1). The good agreement of the calculated

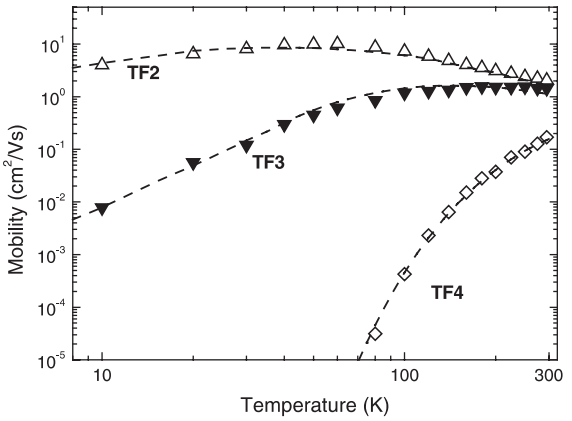

Fig. 7. Comparison of the measured and fitted field-effect mobility for devices TF2–4. The mobility of device TF1 was used as bulk mobility for the calculations. Differences in grain boundary trap densities account for the various temperature dependences (see Table 1).

and measured data suggests that trapping at the grain boundaries is indeed the main cause of the variety of temperature dependences of the field-effect mobility observed in polycrystalline thin film devices. It is worth mentioning that even a very modest variation of the density of trapped charge n_t can result in drastically different $\mu(T)$ curves. The calculated trap densities increase with decreasing deposition temperature of the pentacene thin films. However, further investigations are necessary to shed more light onto the microscopic nature of the trap states.

In addition, the measured on/off-ratio, the sub-threshold swing, and the resistivity decrease with decreasing deposition temperature (see Table 1). The increase in conductivity may well be caused by the incorporation of additional dopants and impurities into the films. As a result of this and due to the decrease of the mobility, the on/off-ratio drops. The increased sub-threshold swing can also be ascribed to an increased number of trapping states.

For samples with high trap densities the mobility also depends on the applied gate voltage. Similar results are found in the literature [24–28]. However, we point out that high quality samples (SX, TF1–2) do not show this gate-voltage dependent μ_{FE}. Therefore we believe that this effect, which is observed in oligothiophene and pentacene thin films, is caused by disorder or trapping and is not an intrinsic property of the material itself. This can be easily seen in the present model as the effective barrier height at the grain boundaries depends on the position of the Fermi level E_F (see Eqs. (4) and (5)) and E_F can be shifted by the applied gate voltage V_g. Consequently, E_B becomes a function of the V_g. Fig. 8 shows the

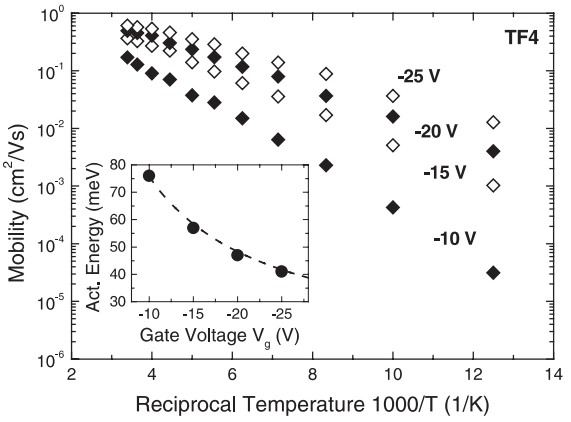

Fig. 8. Field-effect mobility of device TF4 as function of temperature and gate voltage. The inset shows the activation energy as a function of the applied gate voltage.

Table 1
Parameters of pentacene FETs fabricated on a single crystal (SX) and on four different thin films (TF1–TF4): room-temperature mobility μ_{RT}, maximal mobility μ_{max}, sub-threshold swing S, on/off-ratio, conductivity σ, grain boundary trap density n_t, and inversion channel mobility μ_n

	μ_{RT} (cm²/V s)	μ_{max} (cm²/V s)	S (V/decade)	On/off	σ (S/cm)	n_t (cm^{-2})	μ_n (cm²/V s)
SX	3.2	10^5	0.06	10^9	10^{-14}	–	2.0
TF1	2.4	400	0.15	10^8	10^{-12}	–	0.5
TF2	2.1	10	0.3	10^7	10^{-11}	7×10^{10}	2×10^{-3}
TF3	1.4	1.6	0.9	10^6	10^{-9}	3×10^{11}	–
TF4	0.2	0.2	1.5	10^4	10^{-7}	1×10^{12}	–

field-effect mobility of TF4 as function of temperature and applied gate voltage. As the value of V_g increases, the effective carrier density in the p-channel and therefore in the grains rises also, resulting in a screening of the trapped charges and a reduction of the barrier height. In a crude approximation E_B becomes proportional to $1/V_g$ (see inset of Fig. 8) [19,20].

3.3. Electron accumulation

Pentacene FETs can also exhibit n-channel activity [10], i.e. the formation of an electron accumulation layer, in addition to the frequently observed p-type transistor action. Fig. 9 shows the temperature dependence of the n-channel mobility of devices SX, TF1 and TF2. The mobility of transistor SX increases from 2 cm^2/Vs at room temperature following a power law up to 10^4 cm^2/Vs at low temperatures, typical for band-like charge transport. At room temperature an on/off-ratio of 10^8 and a sub-threshold swing of 150 mV/decade are measured. The less steep sub-threshold characteristics suggests that more electron traps than hole traps are present in this material or at the pentacene/Al_2O_3 interface. This becomes even more obvious for thin film devices. Only devices TF1 and TF2 exhibited n-channel activity. Operation in inversion is suppressed in TF3 and TF4 by effective electron trapping. Moreover, the electron mobility in TF1 is thermally activated, which is in contrast to p-channel transport, where 'intrinsic' band-like motion was observed. Device TF2 exhibits an even lower electron mobility than TF1 with a higher activation energy. Nevertheless, ambipolar FETs can also be prepared from pentacene thin films.

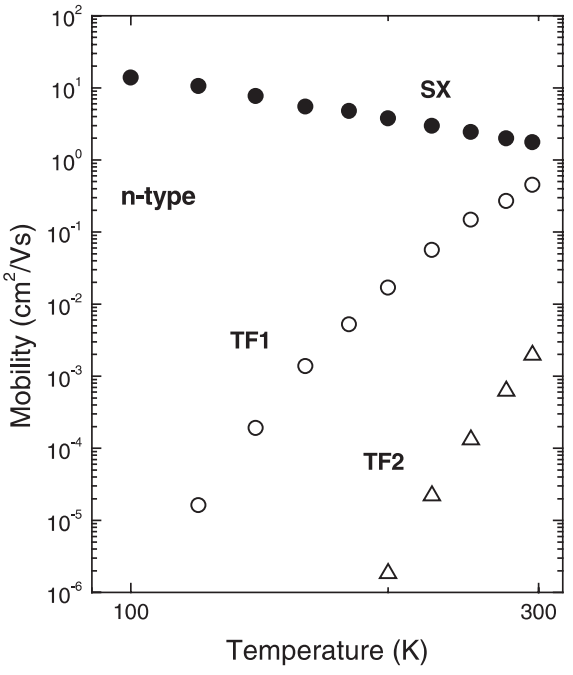

Fig. 9. Temperature dependence of the n-channel field-effect mobility of pentacene single crystal (SX) and thin film transistors (TF1/TF2).

4. Discussion

The performance of single crystalline FETs can be seen as the intrinsic limit for thin film devices, since additional disorder, grain boundaries or traps will reduce mobility, on/off-ratio and sub-threshold swing. The hole mobility of single crystal devices increases with decreasing temperature following a power law. The observed temperature dependence ($T^{-2.7}$) suggests band-like transport, limited by phonon scattering [15,16]. At low temperatures (below 10 K) μ_B seems to be limited by scattering at impurities. In thin film devices the mobility appears to be dominated by grain boundary effects. However, at room temperature mobilities similar to single crystals can be achieved, since the barrier height at the grain boundaries is sufficiently low. Hence, in contrast to conventional inorganic semiconductors nearly 'intrinsic' mobilities can be reached for applications [4,5]. For example, room temperature mobilities in single crystalline Si FETs exceed the values in polycrystalline Si or even amorphous Si by far [14,29,30].

Besides the field-effect mobility the on/off-ratio is another important parameter for applications. This quantity depends on the conductivity, mobility, as well as the geometry of the device [25],

$$\frac{I_{on}}{I_{off}} = \left(\frac{\mu}{\sigma}\right)\frac{C_i^2 V_d^2}{eN_a d}, \tag{6}$$

where σ is the conductivity, N_a the acceptor density, and d the thickness of the semiconductor. C_i is the capacitance per area of the insulator and V_d the drain–source voltage. Although the conductivity of the thin films slightly increases due to additional, extrinsic dopants, on/off ratios of 10^6 can been achieved, high enough for transistor applications.

Furthermore, the single crystal device data demonstrate that sub-threshold swings S even steeper than 150 mV/decade can be possible in thin film transistors by improving the interface between pentacene and the gate insulator. We assume that the difference in S originates from trapped charges at the interface, at grain boundaries, or intragrain defects [29]. It has been shown that the use of self-assembled monolayers, such as octadecyltrichlorosilane, can significantly improve the sub-threshold behavior of organic FETs [31–33]. A further reduction of interface states could improve the sub-threshold characteristics of thin film devices. Nevertheless, a detailed understanding of the microscopic origin of interface states and other defects in thin films seems to be essential for further improvement.

In order to achieve ambipolar transistor action special care has to be taken to minimize electron trapping in the pentacene bulk, at the pentacene/insulator interface, and at grain boundaries. While the microscopic origin of the trap levels is not clear yet, preliminary studies suggest that they are related to oxygen. Furthermore, the use of gold electrodes for electron transport might not be optimal in FETs [34]. We have also used low work-function metals, such as magnesium or aluminum, as electron injecting drain and source electrodes and resulting in similar, slightly higher, electron mobility values in single crystals. The mobility increases from 2.2 $cm^2/V\,s$ at room temperature up to 3×10^4 $cm^2/V\,s$ at lowest temperatures. A detailed understanding of the trapping processes and the charge injection seems to be necessary in order to improve ambipolar transport in thin film devices.

5. Conclusion

The charge transport in pentacene-based single crystalline and polycrystalline FETs has been studied. In thin film devices grain boundaries significantly influence the temperature dependence of the field-effect mobility. At room temperature, however, values close to the intrinsic limit (>2 $cm^2/V\,s$) can be achieved, which is very important for potential applications. Moreover, ambipolar transistor action can be achieved in single crystal devices as well as high quality thin film transistors. The use of ambipolar thin film devices might lead to a significant simplification complementary logic circuits, since no organic material has to be patterned.

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